WHAT IS CLAIMED IS:

1. In a digital signal encoder for encoding first and second digital signals at an encoding clock rate over a frequency band comprising a pilot frequency component, a pilot frequency signal generator comprising:

a phase detector for generating a first output signal representing a phase relationship between a two-state input reference signal and a rollover signal;

a digital loop filter for processing the first output signal to generate an offset term;

a local phase generator for generating the rollover signal that is fed back to the phase detector and for generating an output phase signal based upon the offset term; and

a sinusoid generator for receiving the output phase signal and generating a digital pilot frequency signal that is frequency locked to the input reference signal;

wherein the pilot frequency signal generator operates at a generator clock rate that is substantially higher than the encoding clock rate.

2. The pilot frequency signal generator of claim 1, wherein the phase detector comprises an up/down counter for outputting an indication of the phase relationship between the rollover signal and reference signal.

3. The pilot frequency signal generator of claim 1, wherein the digital loop filter comprises a proportional plus integrator digital filter for scaling the first output signal to generate a sum of a linear term and an integrator term.

4. The pilot frequency signal generator of claim 3, wherein the proportional plus integrator digital filter comprises a cascade of two programmable stages.

5. The pilot frequency signal generator of claim 1, wherein the pilot frequency signal generator is formed on a common substrate with a BTSC encoder circuit.

6. The pilot frequency signal generator of claim 5, wherein the pilot frequency signal generator is fabricated according to standard CMOS processing.

7. The pilot frequency signal generator of claim 1, further comprising a down sampler for converting the digital pilot frequency signal to a converted signal with an equal frequency having a sampling rate equal to the encoding clock rate.

8. The pilot frequency signal generator of claim 7, wherein a compensating term is selectively added to the local phase generator output when the generator clock rate is not an integer multiple of the encoding clock rate.

9. The pilot frequency signal generator of claim 1, wherein the digital loop filter comprises a first saturator for limiting the value of the offset term.

10. A digital integrated circuit BTSC signal encoder for encoding audio signals associated with a video signal, comprising:

(A) matrix means for receiving a first digital audio signal and a second digital audio signal, comprising means for summing said first and second digital audio signals and thereby generating a digital sum signal, and including means for subtracting one of said first and second digital audio signals from the other of said digital first and second digital audio signals and thereby generating a digital difference signal;

(B) sum channel processing means for processing said digital sum signal;

(C) difference channel processing means for digitally processing said digital difference signal; and

(D) a pilot generator for producing a digital sinusoid that is frequency-locked to a two-state input reference signal whose repetition rate is equal to a horizontal scan rate of the video signal;

wherein the sum channel processing means and the difference channel processing means operate at a first sample rate to substantially match BTSC analog filter transform functions in both magnitude and phase, and the pilot generator operates at a second sample rate that is higher than the first sample rate.

11. The BTSC signal encoder of claim 10, wherein the pilot generator comprises a counter, a digital loop filter, a pilot frequency offset adder, a phase accumulator for generating a feedback signal and a phase signal, and a sinusoidal generator, where the counter detects and outputs a phase relationship between the

input reference signal and the feedback signal, the digital loop filter generates an offset value, the adder adjusts an expected pilot frequency by the offset value, and the sinusoidal generator comprises a look-up table.

12. The BTSC signal encoder of claim 11, wherein the counter comprises a four bit up/down counter and the digital loop filter comprises a digital filter for scaling the counter output.

13. The BTSC signal encoder of claim 11, wherein the digital loop filter comprises a first digital filter for programmably scaling the counter output to generate a linear term, a second digital filter for programmably scaling and integrating the counter output to generate an integrator term and an adder for summing the linear term and the integrator term.

14. The BTSC signal encoder of claim 10, further comprising a downsampler for converting the digital sinusoid from the second sample rate to the first sample rate.

15. The BTSC signal encoder of claim 10, wherein the first sample rate is at least substantially ten times the bandwidth of the first and second digital audio signals.

16. A method for generating a digital sinusoid signal whose frequency matches the repetition rate of an external reference signal using an internal clock having a first predetermined rate, comprising:

applying a two-state digital reference signal and a feedback signal to a phase detector, where the reference signal is periodic with a repetition rate equal to an external reference frequency;

loop filtering the phase detector output to generate an offset value;

adding the offset value to an expected frequency of the digital sinuosoid to generate a pilot phase signal;

applying the pilot phase signal to a phase accumulator to generate the feedback signal and a phase signal; and

retrieving a digital sinusoid signal corresponding to the phase signal.

17. The method of claim 16, further comprising downsampling the digital sinusoid signal to a second predetermined rate by selecting a subset of the digital sinusoid signal when the first predetermined rate is an integer multiple of the second predetermined rate.

18. The method of claim 16, further comprising downsampling the digital sinusoid signal to a second predetermined rate by selecting a subset of the digital sinusoid signal and adding a compensating term to the phase accumulator output when the first predetermined rate is not an integer multiple of the second predetermined rate.

19. The method of claim 16, further comprising downsampling the digital sinusoid signal to a second predetermined rate.

20. The method of claim 16, wherein the digital sinusoid signal is a BTSC pilot subcarrier that is frequency locked to the horizontal scanning frequency of a transmitted video signal.